What is claimed Is:

1. A method of forming a composite dielectric on a semiconductor substrate, the method comprising:

forming a dielectric layer having an exposed surface on the substrate;

treating the exposed surface of the dielectric layer with phosphine and/or a phosphine plasma; and

forming a cap layer directly on the treated surface of the dielectric layer.

2. The method of claim 1, comprising forming the dielectric by spin-on-glass techniques.

3. The method of claim 1, comprising introducing the substrate to a plasma enhanced chemical vapor deposition (PECVD) chamber having a phosphine source to treat the exposed surface of the dielectric layer.

4. The method of claim 3, comprising introducing phosphine together with a carrier gas to the PECVD chamber as the phosphine source.

5. The method of claim 3, comprising forming the cap layer by PECVD without removing the substrate from the chamber.

6. The method of claim 1, comprising patterning a photoresist on the cap layer and etching through the cap and dielectric layers to expose side surfaces of the cap and dielectric layers.

7. The method of claim 6, comprising subjecting the exposed side surfaces of the cap and dielectric layers to a phosphine plasma.

8. The method of claim 1, comprising forming the dielectric layer from a silsesquioxane dielectric material or derivative thereof.

9. A method of treating a dielectric layer on a semiconductor substrate, the method comprising:

forming a dielectric layer on the substrate;

forming a patterned photoresist on the dielectric layer;

etching through the dielectric layer to expose side surfaces therein; and

subjecting the side surfaces of the dielectric layer to a phosphine plasma.

10. The method of claim 9, comprising

removing the photoresist layer; and

forming a conformal barrier layer on the dielectric layer including the phosphine plasma treated side surfaces thereof.

11. The method of claim 10, comprising forming a conductive layer comprising copper on the conformal barrier layer and within the etched dielectric layer.

12. The method of claim 11, comprising polishing the conductive layer to the barrier layer to form a conductive trench or plug within the dielectric layer.

13. The method according to claim 12, comprising forming a cap layer over the conductive layer and barrier layer.

14. The method according to claim 9, wherein the dielectric layer comprises a porous silicon oxide.

15. The method of claim 14, comprising depositing the silicon oxide at a thickness of about 0.3 microns to about 1 micron.

16. The composite structure according to claim 12.

17. The composite structure according to claim 16, wherein the substrate comprises a single crystal silicon substrate having at least one active device region formed therein or thereon.